CLAIMS

What is claimed is:

1. A semiconductor device where during fabrication the semiconductor device comprises:

a primary layer having a critical dimension specification;

a lower layer over the primary layer, the lower layer subsequently hard mask trimmed to satisfy the critical dimension specification of the primary layer; and

an upper layer over the lower layer, the upper layer having a high-etching selectivity as compared to the lower layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming.

2. The semiconductor device of claim 1, further comprising a thin oxide layer between the lower layer and the primary layer.

3. The semiconductor device of claim 1, wherein the primary layer comprises one of a silicon layer and a polysilicon layer.

4. The semiconductor device of claim 1, wherein the lower layer comprises a dielectric film.

5. The semiconductor device of claim 1, wherein the upper layer comprises a dielectric film.

6. The semiconductor device of claim 1, wherein the lower layer is selected from a group essentially consisting of: Si_3N_4, SiON, and SiO_2.

7. The semiconductor device of claim 1, wherein the upper layer is selected from a group essentially consisting of: polysilicon, Si_3N_4, SiON, and SiO_2.

8. A method for forming a semiconductor device comprising:

patterning a photoresist layer of a semiconductor wafer also having an upper layer under the photoresist layer and over a lower layer, and a primary layer under the lower layer, the primary layer having a critical dimension specification, the upper layer having a high-etching selectivity as compared to the lower layer;

hard mask etching the lower layer and the upper layer;

hard mask trimming at least the lower layer, the lower layer hard mask trimmed to satisfy the critical dimension specification

of the primary layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming; and

removing the upper layer.

9. The method of claim 8, further comprising removing the photoresist layer after hard mask etching and before hard mask trimming.

10. The method of claim 8, further comprising etching the primary layer for shallow trench isolation.

11. The method of claim 8, further comprising:

etching the primary layer for gate formation; and

removing the lower layer.

12. The method of claim 8, the semiconductor wafer also having a thin oxide layer between the lower layer and the primary layer.

13. The method of claim 8, wherein the primary layer comprises one of a silicon layer and a polysilicon layer.

14. The method of claim 8, wherein each of the lower layer and the upper layer comprises a dielectric film.

15. The method of claim 8, wherein the lower layer is selected from a group essentially consisting of: Si_3N_4, SiON, and SiO_2.

16. The method of claim 8, wherein the upper layer is selected from a group essentially consisting of: polysilicon, Si_3N_4, SiON, and SiO_2.

17. A semiconductor device formed at least in part by a method comprising:

patterning a photoresist layer of a semiconductor wafer also having an upper layer under the photoresist layer and over a lower layer, and a primary layer under the lower layer, the primary layer having a critical dimension specification, the upper layer having a high-etching selectivity as compared to the lower layer;

hard mask etching the lower layer and the upper layer;

removing the photoresist layer;

hard mask trimming at least the lower layer, the lower layer

hard mask trimmed to satisfy the critical dimension specification of the primary layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming;

removing the upper layer; and

performing one or more actions selected from the group essentially consisting of:

etching the primary layer for shallow trench isolation; and

etching the primary layer for gate formation and removing the lower layer.

18. The semiconductor device of claim 17, the semiconductor wafer also having a thin oxide layer between the lower layer and the primary layer.

19. The semiconductor device of claim 17, wherein each of the lower layer and the upper layer comprises a dielectric film.

20. The semiconductor device of claim 17, wherein each of the lower layer and the upper layer is selected from a group essentially consisting of: Si_3N_4, SiON, and SiO_2.